PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: David W. Boggs et al.	Examiner: Tuan Dinh
Serial No.: 10/668,745	Group Art Unit: 2841
Filed: September 23, 2003	Docket: 884.942US1

For: METHOD AND APPARATUS FOR PROVIDING AN INTEGRATED PRINTED CIRCUIT BOARD REGISTRATION COUPON

APPEAL BRIEF UNDER 37 CFR § 41.37

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Commissioner for Patents
P.O. Box 1450
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Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on October 1, 2007, from the Final Rejection of claims 1-15 and 28-33 of the above-identified application, as set forth in the Final Office Action mailed on May 11, 2007.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $510.00 which represents the requisite fee set forth in 37 C.F.R. § 41.20(b)(2). The Appellant respectfully requests consideration and reversal of the Examiner's rejections of pending claims.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, INTEL CORPORATION.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present application was filed on September 23, 2003 with claims 1-30. A restriction requirement was mailed October 3, 2005. In a response to the restriction requirement, mailed November 3, 2005, Appellant elected claims 1-20 and 28-30. A non-final Office Action was mailed January 24, 2006. In the response to the non-final Office Action, Appellant added new claims 31-33. The response to the non-final Office Action was mailed April 24, 2006. A Final Office Action (hereinafter "the Final Office Action") was mailed July 26, 2006. Appellant filed a response to the July 26, 2006 Final Office Action on October 10, 2006. An Advisory Action was mailed on October 17, 2006. Appellant filed an RCE on October 26, 2006. Another non-final Office Action was mailed November 17, 2006. Appellant filed a response to the November 17, 2006 non-final Office Action on February 7, 2007. A second Final Office Action was mailed April 30, 2007. Appellant filed a Notice of Appeal October 1, 2007. Claims 1-20 and 28-33 stand rejected, remain pending, and are the subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated April 30, 2007.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Some aspects of the present inventive subject matter include a method and apparatus for providing an integrated printed circuit board (PCB) registration coupon. The invention, set forth in the above-referenced application, provides an apparatus to allow a real-time process or method for testing individual PCBs for minimum inner layer coplanar dielectric spacing violations. A PCB can include vertical vias that carry signals. Certain planes within the PCB need to be spaced from the vias that carry signals to prevent shorting to these planes. For example, if a via is too closely spaced or touching a via that normally carries a signal, the signal will short to ground. The spacing between the via and the plane is called an anti-pad.

According to the background of the invention, there is no real-time process or method established to test a PCB to determine if the anti-pads meet specifications. At the time of the invention, destructive testing in the form of cross-sectional analysis is used to test minimum inner layer coplanar dielectric spacing. In an environment where each PCB is to be tested before populating the board with expensive components, destructive testing is not an option. The aspect of the invention claimed is the device or PCB that is formed to accommodate non-destructive testing.

Independent claim 1 FIGs. 1, 2, and 5 and others. Application page 13, line 26 to page 14, line 14; Application page 5 line 10 to page 7 line 12; and Application page 9, lines 10-26.

Independent claim 1 is directed toward a device (100 of FIG. 1) that includes a first major exterior surface (120 of FIG. 1); a second major exterior surface (520 of FIG. 5), at least one of the first major exterior surface (120 of FIG. 1) and the second major exterior surface (520 of FIG. 5) including a plurality of component mounting pads (such as pads for components 130, 132, 134 of FIG. 1); a signal carrying plated through hole (210 of FIGs. 2–5) terminating at the at least one of the first major surface (120) and the second major exterior surface (520); a pad (214) between the first major surface (120) and the second major surface (520). The signal carrying plated through hole (210) is connected to the pad (217 of FIG. 2). The device also includes an antipad element (219 of FIG. 2) substantially surrounding the pad (217). The device

also includes a plane metallization layer (230 of FIG. 2) within the device (100) substantially surrounding the pad (217) and the antipad (219). The device (100) also includes a plated through hole(220 of FIG. 2) attached to the plane metallization layer (230) and terminating at the at least one of the first major exterior surface (120) and the second major exterior surface (520) including the plurality of component mounting pads. The plated through hole (220) is attached to the plane metallization layer (230), and electrically isolated from the plurality of component mounting pads. The device also includes a circuit tester (550 of FIG. 5) for determining if a current will flow between the pad (217) and the signal carrying via (210), and the plane metallization layer (230) to test the spacing of a plane metallization layer (230) from a signal through hole (210) that passes through the plane metallization layer (230) .

Independent claim 10 FIGs. 1, 2, 5 and 9 and others. Application page 13, lines 6-25; Application page 5 line 10 to page 7 line 12; and Application page 9, lines 10-26.

Claim 10 is directed toward a system (2000 of FIG. 9) that includes a processor (2004 of FIG. 9), a memory (2032 of FIG. 9) communicatively coupled to the processor (2004), and a device (100) associated with at least one of the memory (2032) or the processor (2004). The device 100 further including:

a first major exterior surface (120, 320 of FIGs 1 and 3);

a second major exterior surface (520 of FIG. 5), at least one of the first major exterior surface (120, 320) and the second major exterior surface (520) including a plurality of component mounting pads (such as pads for components 130, 132, 134 of FIG. 1);

a signal carrying plated through hole (210 of FIG. 2) terminating at the at least one of the first major surface (120, 320) and the second major exterior surface (520);

a pad (217 of FIG. 2) between the first major surface (120, 320) and the second major surface (520), the signal carrying plated through hole (210) connected to the pad (217);

an antipad element (219 of FIG. 2) substantially surrounding the pad (217);

a plane metallization layer(230 of FIG. 2) substantially surrounding the pad (217)and antipad (219) within the device (100); and

a plated through hole (220 of FIG. 2) attached to the plane metallization layer (230) and terminating at the at least one of the first major exterior surface (120, 320) and the second major exterior surface (520) including the plurality of component mounting pads (such as pads for components 130, 132, 134 of FIG. 1), the plated through hole (220) attached to the plane metallization layer (230) electrically isolated from the plurality of component mounting pads; and

a circuit test apparatus (550 of FIG. 5) for testing the spacing between the plane metallization layer (230) and the pad (217) associated with the signal carrying through hole (210).

Independent claim 28

28. A device (100 of FIG. 1) including a first major exterior surface (120, 320 of FIGs 1 and 3);

a second major exterior surface (520 of FIG. 5), at least one of the first major exterior surface (120, 320) and the second major exterior surface (520) including a plurality of component mounting pads (such as pads for components 130, 132, 134 of FIG. 1);

a feature (210, 217 of FIG. 2) positioned within the device;

a plated through hole (220 of FIG. 2) attached to a plane metallization layer (230 of FIG. 2) and terminating at the at least one of the first major exterior surface (120, 320) and the second major exterior surface (520) including a plurality of component mounting pads (such as pads for components 130, 132, 134 of FIG. 1), the plated through hole (220) attached to the plane metallization layer (230) within the device (100), and electrically isolated from the plurality of component mounting pads (such as pads for components 130, 132, 134 of FIG. 1), wherein the feature (210, 217) positioned within the device (100) passes through the plane metallization layer (230) and is isolated from the plane metallization layer (230); and

a test device (550) electrically coupled to the feature (210, 217) for testing the spacing between the feature (210, 217) and the plane metallization layer (230).

The summary of the claimed subject matter does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to each of the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether claims 1-9 and 28-33 were properly rejected under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505).

II. Whether claims 10-15 were properly rejected under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690), and further in view of Ott et al. (U.S. 6,147,505)

7. ARGUMENT

A. The Applicable Law under 35 U.S.C. §103(a)

As discussed in *KSR International Co. v. Teleflex Inc. et al.* (U.S. 2007), the determination of obviousness under 35 U.S.C. § 103 is a legal conclusion based on factual evidence. *See Princeton Biochemicals, Inc. v. Beckman Coulter, Inc.*, 7, 1336-37 (Fed. Cir. 2005). The legal conclusion, that a claim is obvious within § 103(a), depends on at least four underlying factual issues set forth in *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17 (1966): (1) the scope and content of the prior art; (2) differences between the prior art and the claims at issue; (3) the level of ordinary skill in the pertinent art; and (4) evaluation of any relevant secondary considerations.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988). To establish a prima facie case of obviousness, three basic criteria should be met. First, there must be some apparent reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *KSR International Co.*, p. 14, line 24 through p. 15, line 8; *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d, 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

The court in KSR made it clear that the Examiner must "determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." Furthermore, "to facilitate review, this analysis should be made explicit." *KSR International Co.*, p. 14, line 24 through p. 15, line 8. KSR made it clear that the Examiner can use a showing of "teaching, suggestion, or motivation" to provide a helpful insight in determining whether the claimed subject matter is obvious under 35 U.S.C. § 103(a). *Id.*. The court in *KSR* also made it clear, however, that the "teaching, suggestion, or motivation" (TSM) test is only one tool that can be used to determine obviousness.

As noted above, to establish a *prima facie* case of obviousness, the Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to

combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *See KSR Int'l Co.*, p. 14, citing *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006); *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002).

In addition, the test for obviousness under §103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir.1985). The Examiner must, as one of the inquiries pertinent to any obviousness inquiry under 35 U.S.C. §103, recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir.1990). The fact that a reference teaches away from a claimed invention is highly probative that the reference would not have rendered the claimed invention obvious to one of ordinary skill in the art. *Stranco Inc. v. Atlantes Chemical Systems, Inc.*, 15 USPQ2d 1704, 1713 (Tex. 1990). When the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious. *Id.* p. 4 citing *United States v. Adams*, 383 U.S. 39, 51-51 (1966). Additionally, critical differences in the prior art must be recognized (when attempting to combine references). *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir.1990).

Furthermore, the Court in *KSR* reaffirmed that "[a] factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of argument reliant upon ex post reasoning." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 82 USPQ2d at 1397. *See also Graham v. John Deere Co.,* 383 U.S. at 36, 148 USPQ at 474.

B. Discussion of the rejections.

B.1 Discussion of the rejection of claims 1-9 and 28-33 under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505).

Appellant timely traversed, asserting that a prima facie case of obviousness had not been established using Shiraki in view of Ott et al.

Claims 1-9

Independent claim 1 recites, among other things, "a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads" and "a circuit tester for determining if a current will flow between the pad and the signal carrying via, and the plane metallization layer to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer".

Appellant respectfully submits that the Examiner has made an improper prima facie showing of obviousness at least because the Examiner's proposed combination of Shiraki and Ott et al. fails to teach or suggest an arrangement "to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer", as recited in claim 1.

The Examiner admits that Shiraki does not teach a circuit tester for determining if a current will flow between the pad and the signal carrying via, and the plane metallization layer to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer. (See page 3 of the Office Action dated April 30, 2007). The Examiner asserts that Ott et al. teaches the missing element. Appellant respectfully disagrees. Ott et al. teaches an adapter arrangement having uniform grid separation of probes to simultaneously test conductive traces of printed circuit boards. Appellant is unable to find in Ott et al. a teaching or suggestion that the adapter arrangement of Ott et al. can be combined with a device, such as the device of Shiraki, to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer of the device, as recited in claim 1. Thus, Appellant respectfully submits that the proposed combination of Shiraki and Ott et al. fails to

teach or suggest at least an arrangement "to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer", as recited in claim 1.

In addition, Appellant is unable to find any motivation for combining Shiraki and Ott et al. as proposed by the Examiner to achieve Appellant's inventive subject matter because neither Shiraki nor Ott et al. teaches an arrangement to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer, as recited in claim 1. Notwithstanding the forgoing, the Examiner appears to use hindsight to propose the combination of Shiraki and Ott et al. based on Appellant's disclosure.

Even if one were to find proper motivation to combine Shiraki and Ott et al., there would be no reasonable expectation of success, as required to make a proper prima facie case of obviousness. Shiraki teaches a grid of equally spaced through-holes 41 that attach to either a power plane metallization layer or a ground plane metallization layer. Shiraki also teaches land 31 connected to the end of the through hole for the signal carrying line. However, land 31 is not spaced on the same grid. Rather, land 31 is spaced between four of the equally spaced through-holes. Thus, in Shiraki, land 31 is not on the grid of equally spaced through-holes. In contrast, Ott et al. specifically teaches a uniform grid separation of the probes. [See abstract of Ott et al. (U.S. 6,147,505)]. Therefore, even if one were to combine Shiraki and Ott et al. as proposed by the Examiner, the equally spaced grid of Ott et al. would not electrically contact land 31 of Shiraki because land 31 is not positioned on a grid. Thus, the proposed combination of Shiraki and Ott et al. would not work.

The reasons presented above demonstrate that the proposed combination of Shiraki and Ott et al. fails to teach or suggest all the limitations recited in claim 1. Even if Shiraki and Ott et al. are combined as proposed by the Examiner, the combination would not work. Therefore, Appellant submits that the Examiner has not established a prima facie case of obviousness in rejecting claim 1. Accordingly, Appellant requests reversal of the rejection and allowance of claim 1. Claims 2-9 depend from claim 1 and include the things of claim 1. Thus, Appellant submits that claims 2-9 are also in patentable condition for at least the reasons present above regarding claim 1. Accordingly, Appellant requests reversal of the rejection and allowance of claims 2-9.

Claims 28-33

Independent claim 28 recites, among other things, "a test device electrically coupled to the feature for testing the spacing between the feature and the plane metallization layer". For the reasons at least similar to those presented above regarding claim 1, Appellant respectfully submits that the Examiner has made an improper prima facie showing of obviousness at least because the Examiner's proposed combination of Shiraki and Ott et al. fails to teach or suggest "a test device electrically coupled to the feature for testing the spacing between the feature and the plane metallization layer", as recited in claim 28. Accordingly, Appellant requests reversal of the rejection and allowance of claim 28. Claims 29-33 depend from claim 28 and include the things of claim 28. Thus, Appellant submits that claims 29-33 are also in patentable condition for at least the reasons present above regarding claim 28. Accordingly, Appellant requests reversal of the rejection and allowance of claims 29-33.

B.2 Discussion of the rejection of claims 10-15 under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690), and further in view of Ott et al. (U.S. 6,147,505).

Appellant timely traversed, asserting that a prima facie case of obviousness had not been established using Shiraki in view of Conn et al. and in further view of Ott et al.

Claims 10-15

Independent claim 10 recites, among other things, "a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads, the plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads" and "a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole".

Appellant respectfully submits that the Examiner has made an improper prima facie showing of obviousness at least because the Examiner's proposed combination of Shiraki, Conn et al., and Ott et al. fails to teach or suggest "a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole", as recited in claim 10.

The Examiner admits that Shiraki and Conn et al. do not disclose a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole. (See page 6 of the Office Action dated April 30, 2007). The Examiner again relies on Ott et al. asserts that Ott et al. teaches the missing element. Appellant respectfully disagrees. As discussed above, Ott et al. teaches an adapter arrangement having uniform grid separation of probes to simultaneously test conductive trances of printed circuit boards. Appellant is unable to find in Ott et al. a teaching or suggestion that the adapter arrangement of Ott et al. can be combined with a device, such as the device of Shiraki or Conn et al., or both, to include a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole, as recited in claim 10. Thus, Appellant respectfully submits that the proposed combination of Shiraki, Conn et al., and Ott et al. fails to teach or suggest "a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole", as recited in claim 10.

In addition, Appellant is unable to find any motivation for combining Shiraki, Conn et al., and Ott et al. as proposed by the Examiner to achieve Appellant's inventive subject matter because none of Shiraki, Conn et al., and Ott et al. teaches "a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole, as recited in claim 10. Notwithstanding the forgoing, the Examiner appears to use hindsight to propose the combination of Shiraki, Conn et al., and Ott et al. based on Appellant's disclosure.

Even if one were to find proper motivation to combine the references, there would be no reasonable expectation of success, as required to make a proper prima facie case of obviousness. As discussed above, Shiraki teaches a grid of equally spaced through-holes 41 that attach to either a power plane metallization layer or a ground plane metallization layer. Shiraki also teaches land 31 connected to the end of the through hole for the signal carrying line. However, land 31 is not spaced on the same grid. Rather, land 31 is spaced between four of the equally spaced through-holes. Thus, in Shiraki, land 31 is not on the grid of equally spaced through-holes. In contrast, Ott et al. specifically teaches a uniform grid separation of the probes. [See

abstract of Ott et al. (U.S. 6,147,505)]. Therefore, even if one were to combine Shiraki, Conn et al., and Ott et al., as proposed by the Examiner, the equally spaced grid of Ott et al. would not electrically contact land 31 of Shiraki because land 31 is not positioned on a grid. Thus, the proposed combination of Shiraki, Conn et al., and Ott et al. would not work.

The reasons presented above demonstrate that the proposed combination of Shiraki, Conn et al., and Ott et al. fails to teach or suggest all the limitations recited in claim 10. Even if Shiraki, Conn et al., and Ott et al. are combined as proposed by the Examiner, the combination would not work. Therefore, Appellant submits that the Examiner has not established a prima facie case of obviousness in rejecting claim 10. Accordingly, Appellant requests reversal of the rejection and allowance of claim 10. Claims 11-15 depend from claim 10 and include the things of claim 10. Thus, Appellant submits that claims 11-15 are also in patentable condition for at least the reasons present above regarding claim 10. Accordingly, Appellant requests reversal of the rejection and allowance of claims 11-15.

SUMMARY

Appellant respectfully submits for the reasons argued above, claims 1-15 and 28-33 were not properly rejected. It is respectfully submitted that the cited art does not render the claims obvious and that the claims are patentable over the cited art. Reversal of the rejections and allowance of the pending claims are respectfully requested.

Respectfully submitted,

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Date 5-1-08 By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 1st day of May 2008.

Amy Moriarty
Name

Signature

8. CLAIMS APPENDIX

1. A device comprising:

a first major exterior surface;

a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;

a signal carrying plated through hole terminating at the at least one of the first major surface and the second major exterior surface;

a pad between the first major surface and the second major surface, the signal carrying plated through hole connected to the pad;

an antipad element substantially surrounding the pad;

a plane metallization layer within the device substantially surrounding the pad and the antipad;

a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads, the plated through hole attached to the plane metallization layer, and electrically isolated from the plurality of component mounting pads; and

a circuit tester for determining if a current will flow between the pad and the signal carrying via, and the plane metallization layer to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer.

2. The device of claim 1 wherein the plane metallization layer is a power plane.

3. The device of claim 1 wherein the plane metallization layer is a ground plane.

4. The device of claim 1 wherein the plane metallization layer is a reference voltage plane.

5. The device of claim 1 further comprising a signal carrying plated through hole which passes though the plane metallization layer within the device and terminates at the component

mounting pad at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads.

6. The device of claim 5 wherein the signal carrying plated through hole which passes though the plane metallization layer is electrically isolated from the plane metallization layer and is connected to the component mounting pad at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads.

7. The device of claim 1 wherein the device forms a printed circuit board.

8. The device of claim 1 wherein the device forms a semiconductor chip.

9. The device of claim 1 wherein the plated through hole is a via.

10. A system comprising:

a processor;

a memory communicatively coupled to the processor; and

a device associated with at least one of the memory or the processor further including:

a first major exterior surface;

a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;

a signal carrying plated through hole terminating at the at least one of the first major surface and the second major exterior surface;

a pad between the first major surface and the second major surface, the signal carrying plated through hole connected to the pad;

an antipad element substantially surrounding the pad;

a plane metallization layer substantially surrounding the pad and antipad within the device; and

a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including

the plurality of component mounting pads, the plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads; and

a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole.

11. The system of claim 10 wherein the device is a printed circuit board.

12. The system of claim 10 wherein the device is a portion of a semiconductor chip.

13. The system of claim 10 wherein the plane metallization layer is a ground plane.

14. The system of claim 10 wherein the plane metallization layer is a power plane.

15. The system of claim 10 wherein the plane metallization layer is a reference voltage plane.

28. A device comprising:

a first major exterior surface;

a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;

a feature positioned within the device;

a plated through hole attached to a plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the plated through hole attached to the plane metallization layer within the device, and electrically isolated from the plurality of component mounting pads, wherein the feature positioned within the device passes through the plane metallization layer and is isolated from the plane metallization layer; and

a test device electrically coupled to the feature for testing the spacing between the feature and the plane metallization layer.

29. The device of claim 28 wherein the feature is an electrical trace.

30. The device of claim 28 wherein the feature is a signal carrying through hole.

31. The device of claim 28 wherein the test device includes a pad on one of the first major surface or the second major surface.

32. The device of claim 28 wherein the test device is a probe from a circuit tester.

33. The device of claim 28 wherein the test device is a circuit tester.

9. EVIDENCE APPENDIX

None.

10. RELATED PROCEEDINGS APPENDIX

None.